POWER-ON RESET CIRCUIT AND METHOD FOR LOW-VOLTAGE CHIPS

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to a power-on reset circuit and a method thereof, and more particularly to a power-on reset circuit for use in a chip with low operation voltage and a method thereof.

Description of the Related Art

In general, there are two methods for generating reset signal at power-on state. One method is to generate the reset signal by a RC delay unit, as shown in the circuit schematic illustration in FIG. 1 and the associated voltage diagram in FIG. 2. The other method is to generate the reset signal by using the threshold voltage of an active device, as shown in the circuit schematic illustration in FIG. 3 and the associated voltage diagram in FIG. 4.

Referring to FIG. 1, the power-on reset circuit includes an RC (resistor & capacitor) voltage divider 11 and a comparator 12. The RC voltage divider 11 includes a resistor 111 and a capacitor 112 and generates an output voltage V_{RC}. The RC voltage divider 11 is connected to a voltage source VDD and a ground 13. The comparator 12 receives an input voltage αVDD proportional to the voltage source VDD and the output voltage V_{RC} of the RC voltage divider 11 and generates a reset signal Reset by comparing V_{RC} with αVDD. At the beginning of power on, voltage $V_{RC} < \alpha$ VDD and the comparator enables the reset signal Reset, such as outputting a High State. Then, when voltage $V_{RC} >= \alpha$ VDD, the comparator disables the

reset signal Reset, such as outputting a Low state. As shown in the clock diagram in FIG. 2, when the power is on, the voltage source VDD outputs a transient voltage having a magnitude increasing from 0 as time elapses. At the beginning of power on, voltage $V_{RC} < \alpha$ VDD and the comparator enables the reset signal Reset. At the time when the condition of ($V_{RC} < \alpha$ VDD) is changed to the condition of ($V_{RC} >= \alpha$ VDD), the reset signal Reset is disabled.

Referring to FIG. 3, a power-on reset circuit includes a resistor - metal oxide semiconductor voltage divider 21 and a comparator 22. The resistor - metal oxide semiconductor voltage divider 21 includes a resistor 211 and a metal oxide semiconductor 212 and generates an output voltage V_{th}. The resistor - metal oxide semiconductor voltage divider 21 is connected to a voltage source VDD and a ground 23. The comparator 22 compares an input voltage αVDD proportional to the voltage source VDD to the threshold voltage V_{th} and generates a reset signal Reset by comparing V_{RC} with αVDD. When the threshold voltage V_{th} is greater than the input voltage α VDD, the comparator 22 enables the reset signal Reset. However, when the threshold voltage $V_{th} <= \alpha$ VDD, the comparator 22 disables reset signal Reset to end the reset state. As shown in FIG. 4, at the beginning of power on, the voltage source VDD outputs a transient voltage having a magnitude increasing from 0 as time elapses. At the beginning, the threshold voltage $V_{th} > \alpha$ VDD, the comparator enables the reset signal Reset. At the moment when the condition of ($V_{th} > \alpha$ VDD) is changed to the condition of ($V_{th} <= \alpha$ VDD), the reset signal Reset is disabled.

However, the above-mentioned conventional power-on reset circuits have the

following drawbacks. Usually, for the RC delay circuit, an external capacitor is needed to have enough delay time. For the circuit with the active device, such as the metal oxide semiconductor, the threshold voltage of the active device tends to be changed with the process variation, environment temperature variation, and other conditions. Thus, the conditions of reset signal being disabled are not consistent and may be changed with the variation of the various environment conditions. Consequently, errors may be caused in which the reset signal cannot be disabled, or is not disabled at the proper time. In addition, as the operation voltage of the IC chip gets lower and lower, the operation voltage VDD gets smaller and smaller. Therefore, when the power is on, the transient voltage variation gets smaller and smaller, and thus the tolerance of the threshold voltage variation gets smaller and smaller. Thus, the conventional power-on reset circuits are not suitable for use in the chip with the low operation voltage.

SUMMARY OF THE INVENTION

It is therefore one of the many object of the invention to provide a power-on reset circuit adapted to low-voltage chips. The reset circuit may be applied to the low operation voltage without causing errors in the reset operation after power-on owing to the process variation or temperature variation.

Another object of the invention is to provide a power-on reset circuit adapted to low-voltage chips. The circuit utilizes a ring oscillator, which provides an oscillation frequency that rises as the transient voltage rises, to control the ON/OFF of the switch, to charge/discharge capacitors, and to generate a first voltage by conversion. The first voltage is compared to a second voltage, which is generated

after the transient voltage is processed by the voltage divider. Then, it is determined whether or not the circuit has to be reset.

According to one aspect of the invention, a power-on reset circuit adapted to a low operation voltage chip includes an oscillator, a frequency detector, and a reset signal output circuit. A power source provides a transient voltage when it is on, and the transient voltage has the magnitude that rises as time elapses. The oscillator is coupled to the power source. The oscillator generates an oscillation signal having an oscillation frequency that increases as the transient voltage increases. The frequency detector is coupled to the power source and the oscillator. The frequency detector outputs a corresponding first output voltage according to the oscillation frequency of the oscillation signal. The reset signal output circuit outputs a reset signal according to the first output voltage. The magnitude of the reset signal is one of a first level and a second level.

According to another aspect of the invention, a power-on reset method applied to a power-on reset circuit is provided. The power-on reset circuit includes an oscillator, a frequency detector, and a comparator. The method includes the steps of: receiving a transient voltage when a power source is on, wherein the magnitude of the transient voltage increases as time elapses; providing a corresponding oscillation signal according to the transient voltage, wherein the oscillation signal has an oscillation frequency that increases as the transient voltage increases; outputting a corresponding first output voltage according to the oscillation signal; comparing the first output voltage to a second output voltage; enabling a reset signal when the first output voltage is greater than the second output voltage; and disabling the reset

signal when the first output voltage is equal to or smaller than the second output voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a schematic illustration of a conventional power-on reset circuit using a RC delay unit.

FIG. 2 shows an associated voltage clock diagram of the conventional power-on reset circuit in FIG. 1.

FIG. 3 shows a schematic illustration of a conventional power-on reset circuit using a threshold voltage of a metal oxide semiconductor.

FIG. 4 shows an associated voltage clock diagram of the conventional power-on reset circuit in FIG. 3.

FIG. 5 shows a schematic illustration of a power-on reset circuit according to an embodiment of the invention.

FIG. 6 shows an associated voltage and frequency clock diagram of the power-on reset circuit according to the embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Referring to FIG. 5, the circuit of the embodiment of the present invention includes an oscillator 31, a frequency detector 32 and a comparator circuit 33. The oscillator 31 can be a ring-oscillator and includes a set of at least three odd-numbered and serially connected inverters 311, and the output terminal of the last inverter is connected to the input terminal of the first inverter. The oscillator 31 may also be a voltage-controlled oscillator (VCO). Each inverter is powered by a voltage source VDD. The oscillator 31 generates an oscillation signal ck. The frequency detector

32 is coupled to the voltage source VDD and a ground 34 and includes a current source 321, a first capacitor 322, a second capacitor 323, a first switch 324 and a second switch 325. The frequency detector 32 outputs a first output voltage V_{FD} according to the oscillation signal ck generated by the oscillator 31. The current source 321 is coupled to the voltage source VDD. The first capacitor 322 has a first terminal coupled to the output terminal of the current source 321, and a second terminal coupled to the ground 34. The second capacitor 323 and the first capacitor 322 are commonly connected to the ground 34. The first switch 324 is coupled to the first terminal of the first capacitor 322 and another terminal of the second capacitor 323. The second switch 325 and the second capacitor 323 are connected in parallel. The comparator circuit 33 includes a resistor - voltage divider 331 and a comparator 332 and generates a reset signal Reset. The resistor - voltage divider 331 is coupled to the voltage source VDD and generates a second output voltage αVDD proportional to the voltage source VDD with a first resistor 3311 and a second resistor 3312. The comparator 332 compares the first output voltage V_{FD} to the second output voltage αVDD. When the first output voltage V_{FD} is greater than the second output voltage αVDD, the comparator 332 enables the reset signal Reset, such as outputting a High state; and when the first output voltage V_{FD} is smaller than or equal to the second output voltage αVDD, the comparator 332 disables the reset signal Reset, such as outputting a Low state.

In this embodiment, when the power is on, the voltage source VDD is at a transient voltage having the magnitude that increases from 0 as time elapses. The oscillation frequency of the oscillation signal ck of the oscillator 31 increases with

the rising of the transient voltage. The oscillation frequency thereof also decreases with the increasing of the number of the cascaded inverters in the oscillator 31. Thus, the magnitude of the transient voltage input to the inverters and the number of the cascaded inverters will determine the oscillation frequency of the oscillation signal ck. In the frequency detector 32, the switching operations of the first switch 324 and the second switch 325 are controlled by the oscillation signal ck. The state of the first switch 324 is opposite to that of the second switch 325. That is, when the first switch 324 is ON, the second switch 325 is OFF and vice versa. Therefore, the ON/OFF states of the first switch 324 and the second switch 325 alternate with the oscillation frequency of the oscillation signal ck and the switching states of the first switch 324 and the second switch 325 are different.

In the circuit implementation of this embodiment, the first switch 324 substantially switches according to the oscillation signal ck while the second switch 325 substantially switches according to an inverse signal of the oscillation signal ck, as shown in FIG. 5. The frequency detector 32 has a current source 321 and two capacitors 322, 323 coupled in parallel via the first switch 324. When the states of the first switch 324 and the second switch 325 alternate with the oscillation signal ck, the current source 321 charges/discharges the first/second capacitor 322/323 according to the states of the first switch 324 and the second switch 325, respectively. When the oscillation frequency of the oscillation signal ck is lower, the charge/discharge time of the first/second capacitor 322/323 is longer. In this case, the magnitude of the first output voltage V_{FD} approximates the transient voltage of the voltage source VDD. When the oscillation frequency of the oscillation signal

ck is higher, the charge/discharge time of the first/second capacitor 322/323 is shorter. In this case, the first output voltage V_{FD} is smaller than the transient voltage of the voltage source VDD, and decreases with the increasing of the oscillation frequency of the oscillation signal ck. If the current of the current source 321 in the frequency detector 32 is I, and the first capacitor 322 has a capacitance C_1, the second capacitor 323 has a capacitance C_2, the oscillation signal ck has an oscillation frequency f_{ck}, then the magnitude of the first output voltage V_{FD} generated by the frequency detector 32 is:

$$V_{FD} = (I/f_{ck})*((2*C_1+C_2)/(C_1*C_2)).$$

According to the above-mentioned equation, the first output voltage V_{FD} of the frequency detector 32 is inversely proportional to the oscillation frequency f_{ck} of the oscillation frequency ck. So, when the value f_{ck} of the oscillation frequency ck is higher, the first output voltage V_{FD} is lower.

Since the operation principle and manner of the comparator circuit 33 are similar to those of the conventional power-on reset circuit, detailed description thereof may be found in the above-mentioned description and will be omitted.

It is to be noted that in this invention, the comparator circuit 33 also may be implemented by an inverter. The inverter receives the first output voltage V_{FD} and determines the level of the output reset signal according to the magnitude of the first output voltage V_{FD}. When the power source is just started, the value of the first output voltage V_{FD} is smaller than a default threshold value of the inverter. At this time, the inverter regards the first output voltage V_{FD} as a low-level signal and inversely outputs a high-level signal to enable the reset signal Reset. Because the

value of the first output voltage V_{FD} increases as time elapses, when the value of the first output voltage V_{FD} is greater than the default threshold value of the inverter, the inverter regards the first output voltage V_{FD} as a high level signal and inversely outputs a low-level signal to disable the reset signal Reset. In this embodiment, the working principle of the power-on reset circuit in FIG. 3 is illustrated in FIG. 6.

The oscillation frequency of the oscillation signal ck output from the oscillator 31 relates to the magnitude of the voltage source VDD. When the voltage source VDD is lower, the oscillation frequency f_{ck} of the oscillation signal ck output from the oscillator 31 is also lower. According to the above-mentioned equation for the first output voltage V_{FD}, the first output voltage V_{FD} approximates to the voltage source VDD, so the first output voltage V_{FD} is greater than α VDD. When the first output voltage V_{FD} is greater than α VDD, the comparator 332 enables the reset signal Reset. At this time, the digital circuit that needs to be reset on the chip is in a reset state. With the rising of the voltage source VDD, the oscillation frequency f_{ck} of the oscillation signal ck increases. In this case, the first output voltage V_{FD} gradually decreases. When the first output voltage V_{FD} decreases to be smaller than or equal to α Vdd, the comparator 332 disables the reset signal Reset. That is, the reset is disabled while the digital circuit may start to work. In practice, in the above-mentioned circuit, the current source 321 may be replaced by a resistor, the comparator 332 also may be replaced by an inverter to make the circuit operable under a lower operation voltage.

While certain exemplary embodiments have been described and shown in the accompanying drawings, it is to be understood that such embodiments are merely

illustrative of and not restrictive on the broad invention, and that this invention not be limited to the specific construction and arrangement shown and described, since various other modifications may occur to those ordinarily skilled in the art.